

Thank you for taking the Week 10 : Assignment 10.

Course outline

How does an NPTEL online course work?

Week 0

Week 1

Week 2

Week 3

Week 4

Week 5

Week 6

Week 7

Week 8

Week 9

Week 10

Lecture 48: DIRECT MEMORY ACCESS

Lecture 49: SOME EXAMPLE DEVICE INTERFACING

Lecture 50: EXERCISES ON

Week 10 : Assignment 10

Your last recorded submission was on 2021-10-05, 17:17 IST

Due date: 2021-10-06, 23:59 IST.

- 1) Consider the following statement:
 (i) In programmed I/O several instructions are executed for transfer of each word of data.
 (ii) Programmed I/O is not suitable for high-speed data transfer.
 Which of the following is correct?

1 point

- a. Only (i) is true.
- b. Only (ii) is true.
- c. Both (i) and (ii) are true.
- d. Both (i) and (ii) are false.

- a.
- b.
- c.
- d.

- 2) Consider a programmed I/O system where 20 instructions are required to be executed for the transfer of each word of data. The cycles-per-instruction (CPI) of the machine is 1.5 and the processor clock frequency is 2 GHz. The maximum data transfer rate will be _____ million words per second. (Assume 1 million = 10^6)

66.67

1 point

I/O TRANSFER

Lecture 51: BUS STANDARDS

Lecture 52: Universal Serial Bus (USB)

Week 10 Lecture Material

Quiz: Week 10 : Assignment 10

Feedback form for Week 10

Week 11

DOWNLOAD VIDEOS

Assignments Solution

Live Interactive session

Text Transcripts

Books

3) Which of the following statement(s) is/are true for DMA data transfer? 1 point

- a. Data transfer requires very less CPU intervention.
- b. Suitable for transferring large blocks of data
- c. Allow direct data transfer between I/O and memory.

a.

b.

c.

4) Suppose the rotating speed of disk is 36000 rpm, with average rotational delay of 10 msec, suppose there are 512 Kbytes of data recorded in every track. Once the disk head reaches the desired track, the sustained data transfer rate will be Mbyte/sec.

51.2

1 point

5) Which of the following registers needs to be initialized before transfer of any data in DMA mode? 1 point

- a. Memory address
- b. Word count
- c. Address of data on disk
- d. None of these.

a.

b.

c.

d.

1 point

6) Consider the following statements for Bus implementation:
(i) Bus width defines number of wires available in the bus for transferring data.
(ii) Bus bandwidth defines the total amount of data that can be transferred over the bus per unit of time.

- a. Only (i) is true
- b. Only (ii) is true
- c. Both (i) and (ii) are true
- d. Both (i) and (ii) are false

- a.
- b.
- c.
- d.

1 point

7) Consider a matrix keyboard consisting of 256 keys, organized as 16 rows and 16 columns. How many port lines will be required to interface the keyboard?

- a. 256
- b. 128
- c. 64
- d. 32

- a.
- b.
- c.
- d.

8) Suppose that it is required to transfer 20K bytes in interrupt-driven mode of data transfer. Every time an interrupt occurs, it involves the transfer of 64 bytes of data that takes 20 microseconds for the processor to service. The time required to transfer 20K bytes of data will be milliseconds? (Assume 1K = 1024)

6.4

1 point

9) Which of the following is/are advantage of serial bus over parallel bus?

1 point

- a. Low implementation cost
- b. High speed
- c. No interference
- d. All of these

- a.
- b.
- c.
- d.

10) The maximum data transfer rates supported by USB 1.1 and USB 3.0 standards are respectively:

1 point

- a. 12 Gbps and 50 Gbps
- b. 12 Mbps and 5 Gbps
- c. 5 Gbps and 10 Gbps
- d. 2 Gbps and 10 Gbps

- a.
- b.
- c.
- d.

You may submit any number of times before the due date. The final submission will be considered for grading.

Submit Answers

Note: All these answers are confirmed from our side, we don't guarantee that you will get a 100% score. These are our own answers that we are sharing with you all. If you have any doubt that our answers are not correct then feel free to discuss (in-group) or do your own answer.

Most important: We don't promote any type of cheating, these answers are only for those students who are not able to do it on their own or need some help.